先進顯示與光電子技術
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香港科技大學
THE HONG KONG
UNIVERSITY OF SCIENCE
AND TECHNOLOGY

A Cost-Effective Fluorination Method for Enhancing the Performance of Metal Oxide Thin-Film Transistors Using a Fluorinated Planarization Layer

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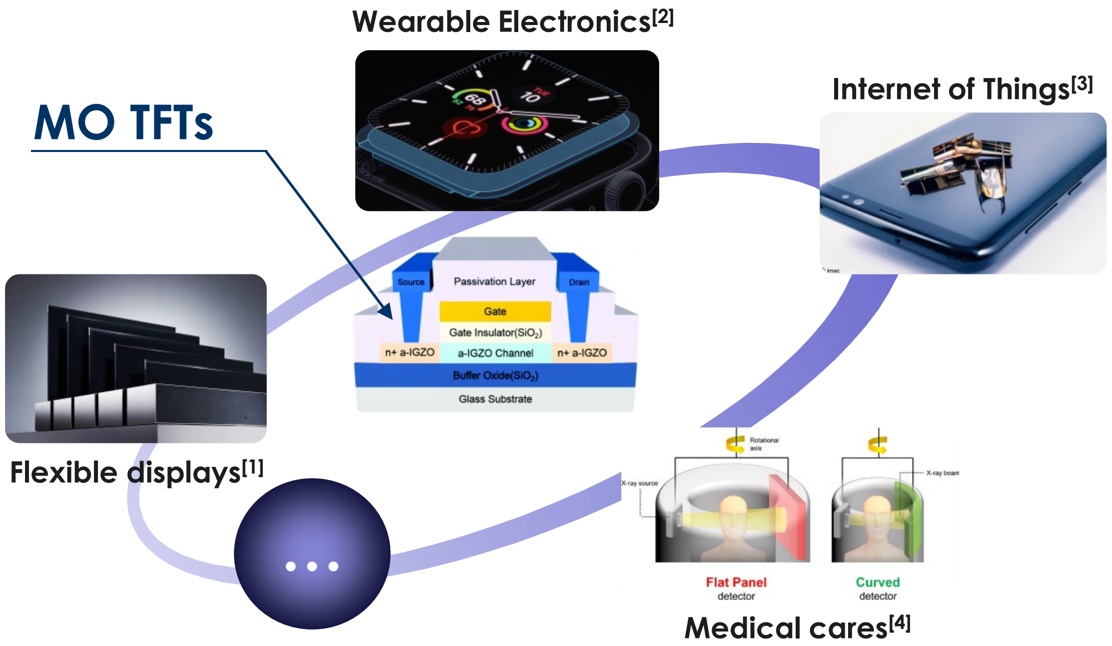
Outline

1. Introduction
2. Unanticipated ΔV_{th} in Top-Gate (TG) Metal-Oxide (MO) TFTs after Planarization (PLN)
3. Fluorination Treatment on Bottom-gate (BG) MO TFTs via PLN
4. Conclusion

MO TFTs with Instability Issues



MO TFTs

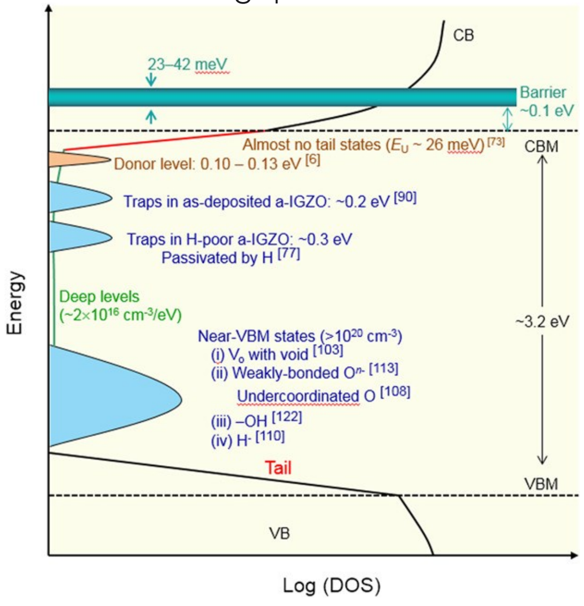
Wearable Electronics[2]

Internet of Things[3]

Flexible displays[1]

Medical cares[4]

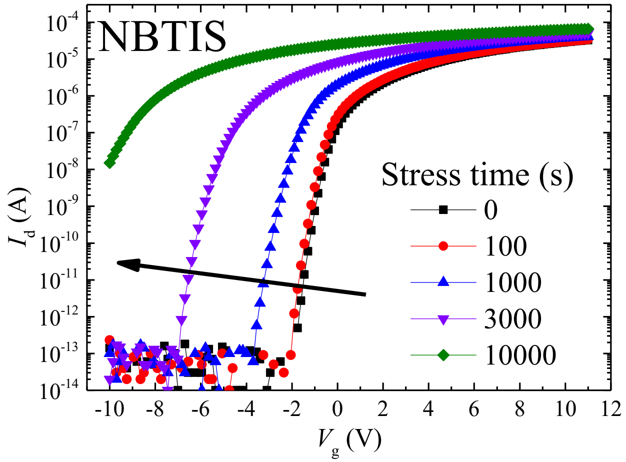
Known electronic structure of a-IGZO with subgap defects[5]



Main defect forms:

- Oxygen vacancy/deficiency
- Weakly-bonded/ undercoordinated oxygen
- Peroxide
- Low valence state cations
- Hydrogen
- Macroscopic structural defects

A typical V_{th} shift degradation occurred during stress



Stretched-exponential equation:

$$\Delta V_{th} = \Delta V_{\infty}\left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right]$$

Stretched-exponential factor

Threhold voltage shift

Extrapolated "saturation" shift

Trapping time constant

Stress time

[1] LG Electronics' SIGNATURE website

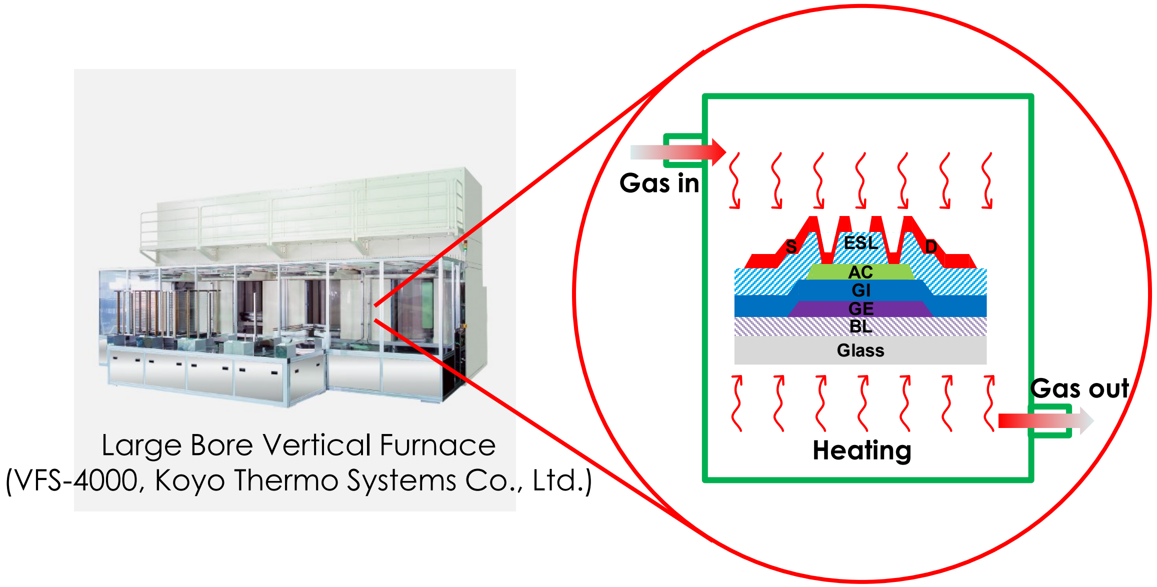
[2] Apple YouTube Channel

[3] IMEC press release

[4] van Breemen, et al. *npj Flex. Electron.* 4.1 (2020): 1-8.

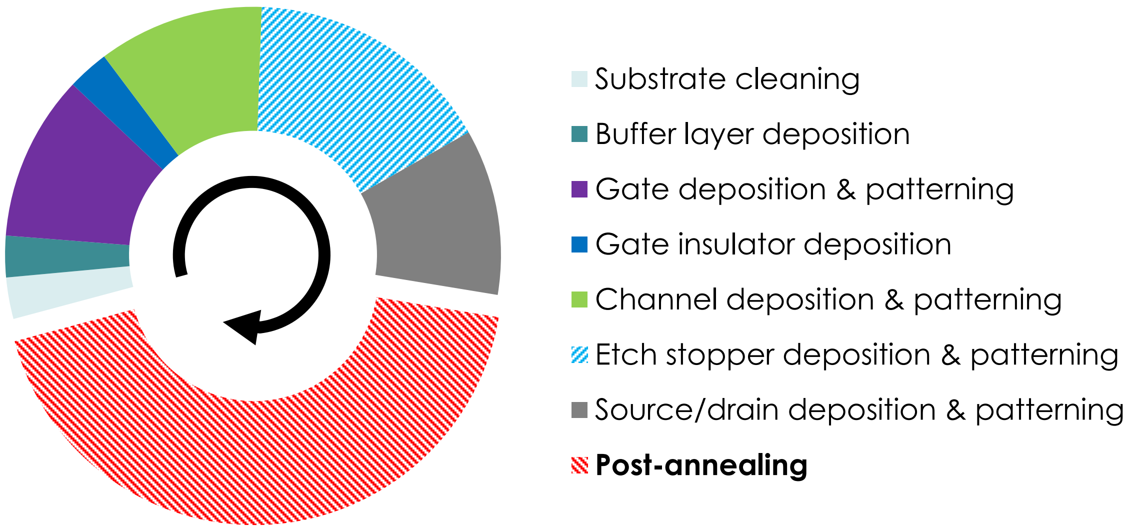
[5] Ide, Keisuke, et al. *Phys. Status Solidi (a)* 216.5 (2019): 1800372.

Thermal Annealing/Oxidation for MO TFTs



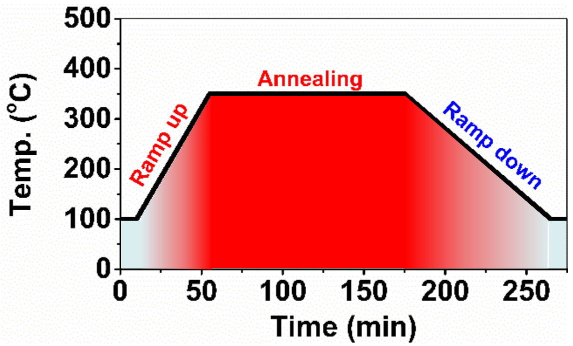
Large Bore Vertical Furnace
(VFS-4000, Koyo Thermo Systems Co., Ltd.)

A typical process flow of ESL MO TFTs in HKUST



Positive impacts of thermal annealing[1]:

- Oxygen vacancy compensation
- Weakly bonded species removal
- Donor level and conductivity control
- Structural relaxation
- Etc.



❖ High annealing temperature & Long annealing time

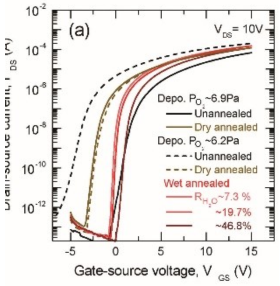
→ Large thermal budget

→ **NOT** cost-effective

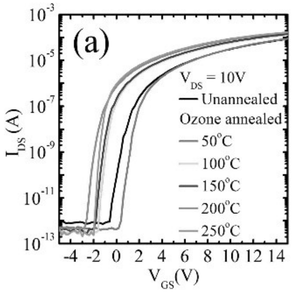
[1] Ide, Keisuke, et al. *Phys. Status Solidi(a)* 216.5 (2019): 1800372.

Advanced Annealing/Oxidation Techniques

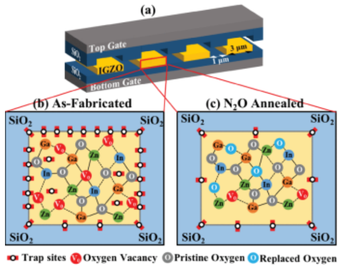
- **Annealing in different gases**[1]-[3]



Wet oxygen

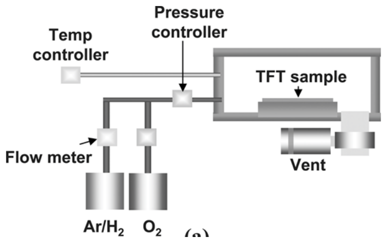


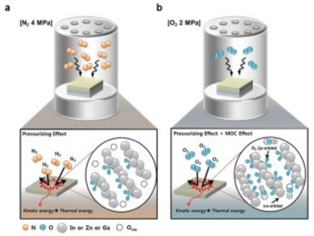
Ozone



Nitrous oxide

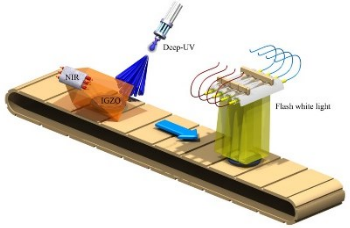
- **High-pressure annealing**[4][5]



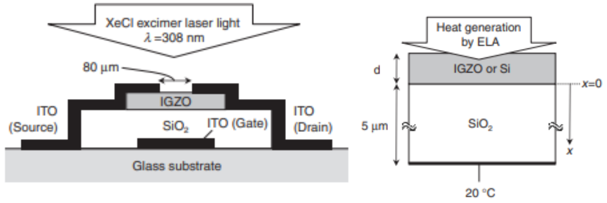


Annealing atmospheres

- **Irradiation assisted annealing**[6][7]

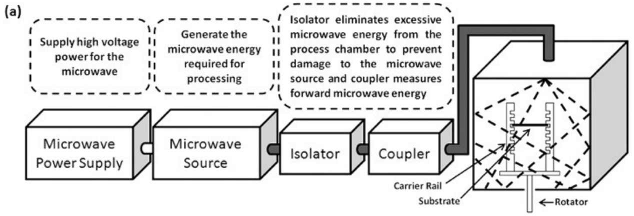


Lamp (DUV, Xenon, Halogen, Flash white light, etc.)

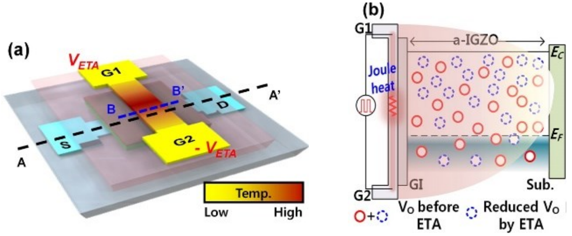


Laser (excimer, CO_2, etc.)

- **Microwave assisted annealing**[8]



- **Electrically assisted annealing**[9]



Annealing methods

[1] Nomura, Kenji, et al. *Appl. Phys. Lett.* 93.19 (2008): 192107.
[2] Ide, Keisuke, et al. *Appl. Phys. Lett.* 99.9 (2011): 093507.
[3] Rabbi, Md Hasnat, et al. *IEEE Electron Device Lett.* 41.12 (2020): 1782-1785.
[4] Yeob Park, Se, et al. *Appl. Phys. Lett.* 100.16 (2012): 162108.
[5] Kim, Won-Gi, et al. Sci. Rep. 6.1 (2016): 1-7.
[6] Moon, Chang-Jin, et al. *ACS Appl. Mater. Interfaces* 11.14 (2019): 13380-13388.
[7] Nakata, Mitsuru, et al. *Jpn. J. Appl. Phys.* 48.11R (2009): 115505.
[8] Teng, Li-Feng, et al. *Appl. Phys. Lett.* 101.13 (2012): 132901.
[9] Kim, Choong-Ki, et al. *ACS Appl. Mater. Interfaces* 8.36 (2016): 23820-23826.

✓ Lower annealing temperature and shorter annealing time
→ Reduced thermal budget

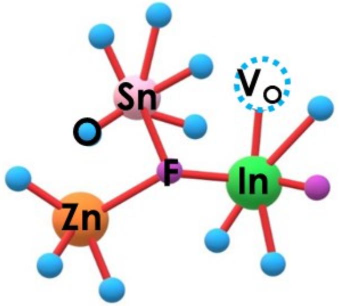
❖ Include additional facility and new materials in existing production lines
→ **NOT** cost-effective

Fluorination Treatments for MO TFTs

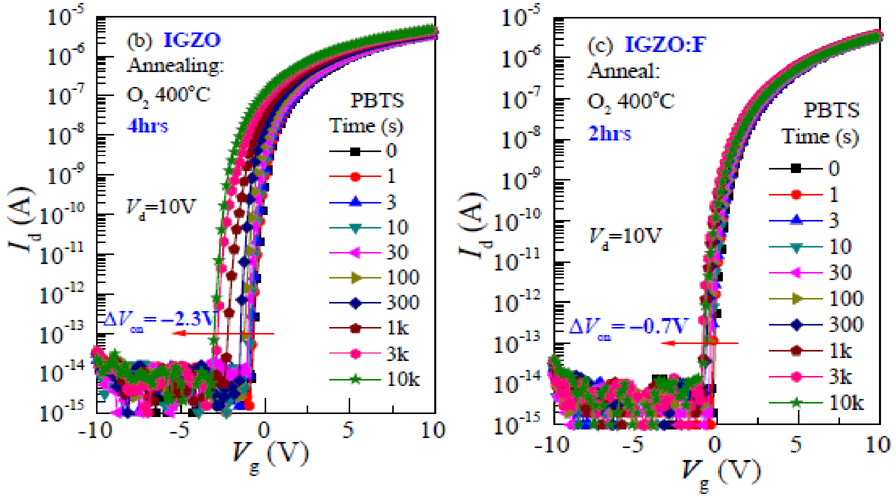
- Fluorine: the largest electronegativity (3.98) among all elements.[1]
- Bond-dissociation energy (D_0): D_0(In-F)= 516 kJ/mol or 5.327 eV **>** D_0(In-O) = 346 kJ/mol or 3.586 eV[2]

✓ Fluorination is more efficient to passivate oxygen vacancy sites than thermal annealing/oxidation

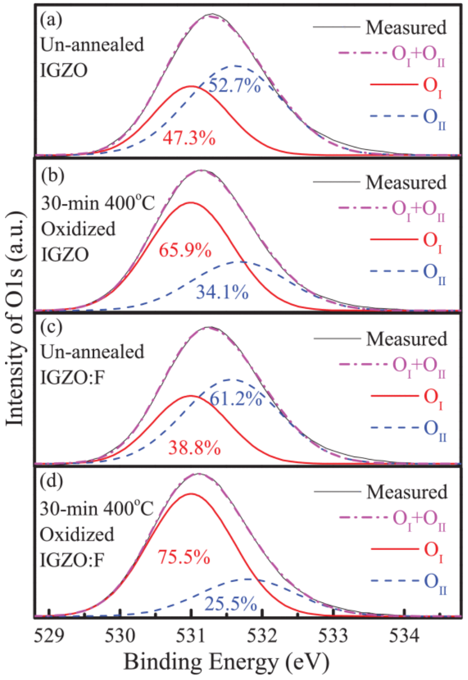
→ Better device stability & less thermal budget.



PBTS-induced transfer curves shift of IGZO and IGZO:F TFTs in HKUST[3]



XPS spectra of O1s for IGZO and IGZO:F[3]



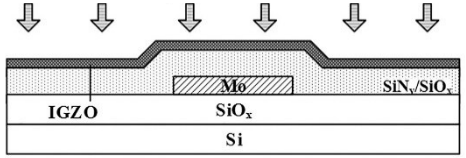
❖ However, many prevalent fluorination treatments are performed under relatively harsh conditions.

→ Physical bombardments on MO channels, result in SS deterioration and newly emerged instability issues.

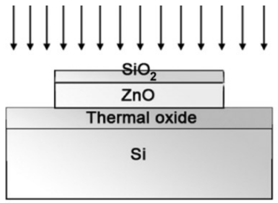
❖ Additional fluorination steps are inserted into the existing process flows

→ **NOT** cost-effective

F-containing (CF_4, SF_6, CHF_3, etc.) Plasma Immersion[4]



Fluorine Implantation[5]

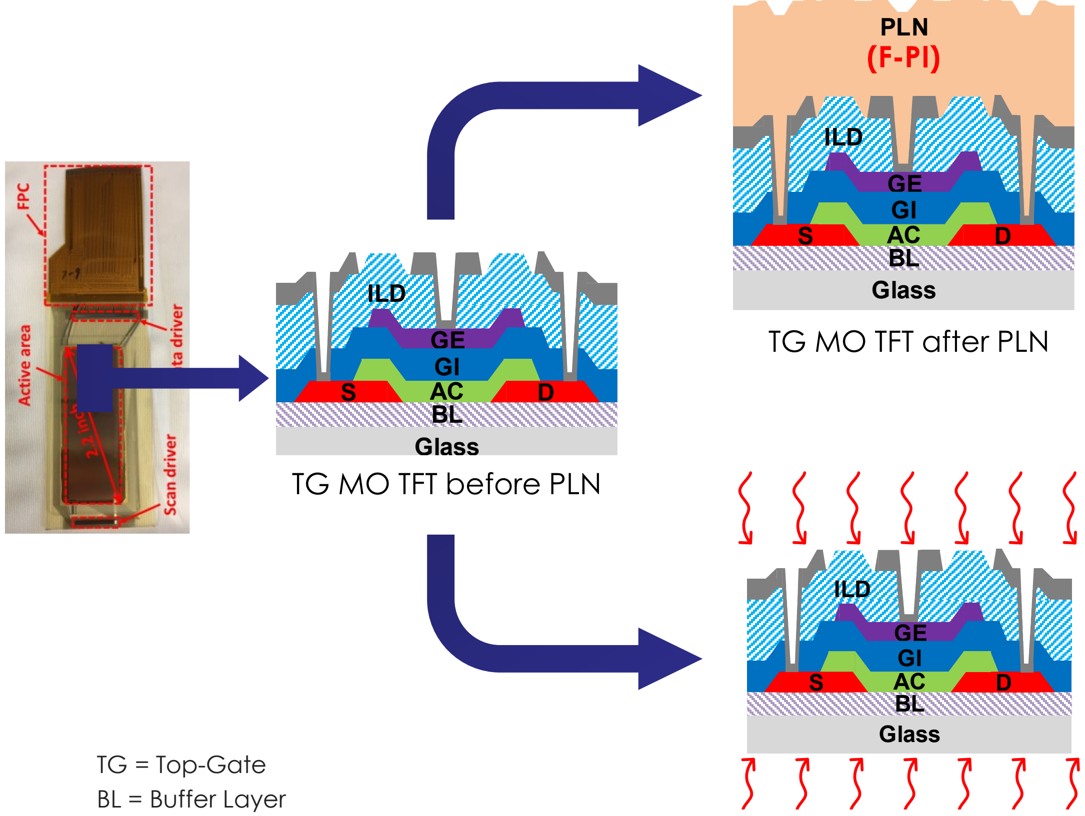


Any other favorable fluorination methods?

[1] Jung, Kyung-Mo, et al. *J. Phys. D*. 53.35 (2020): 355107.
[2] Miyakawa, Masashi, et al. *AIP Adv*. 10.6 (2020): 065004.
[3] Lu, Lei, et al. *IEEE Electron Device Lett*. 39.2 (2017): 196-199.
[4] Wang, Sisi, et al. *J. Soc. Inf. Disp*. 28.6 (2020): 520-527.
[5] Ye, Zhi, et al. *IEEE Electron Device Lett*. 33.4 (2012): 549-551.

Unanticipated ΔV_{th} in TG MO TFTs after PLN (I)

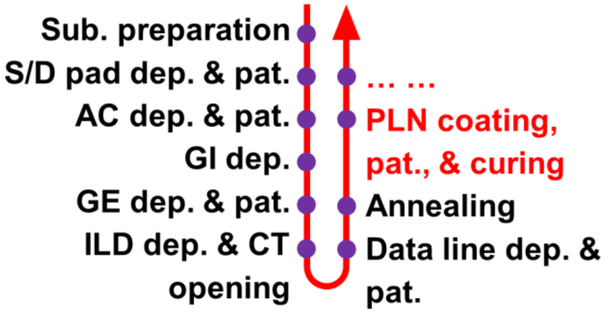
- **Before PLN vs. after PLN**

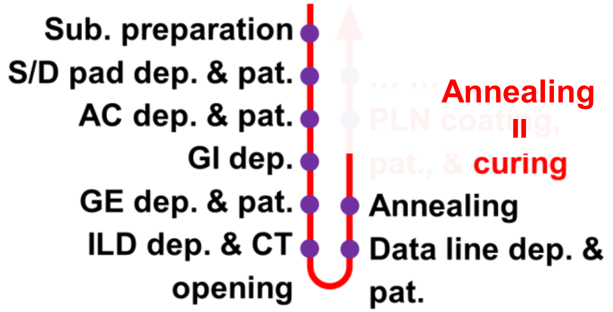


TG MO TFT after PLN

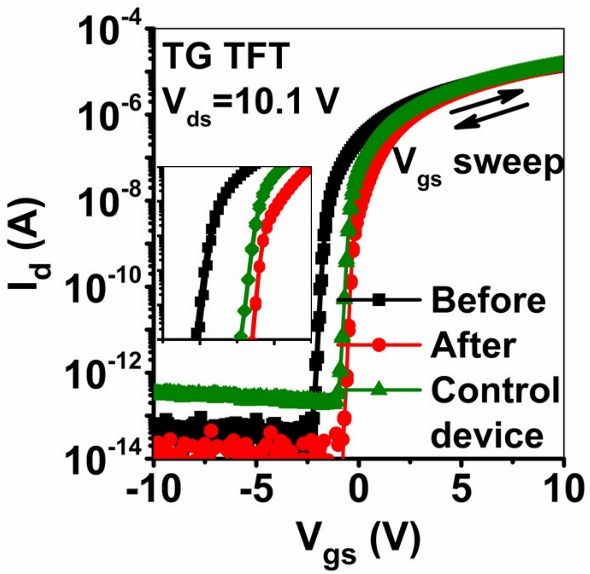
TG MO TFT before PLN

Control device





Electrical performance of TG MO TFTs before/after PLN and control device



	TFT before PLN	TFT after PLN	Control Device
V_{th} (V)	-1.4	0.15	-0.4
ΔV_{th} (V)	-	1.55	1

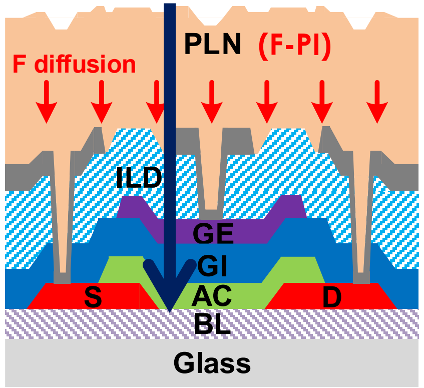
TG = Top-Gate
BL = Buffer Layer
S/D = Source/Drain
GI = Gate Insulator
AC = Active Channel
GE = Gate Electrode
ILD = Inter-Layer Dielectric
PLN = Planarization
F-PI = Fluorinated Polyimide

✓ Not only the curing step but also the F-PI PLN layer is helpful for improving device performance.

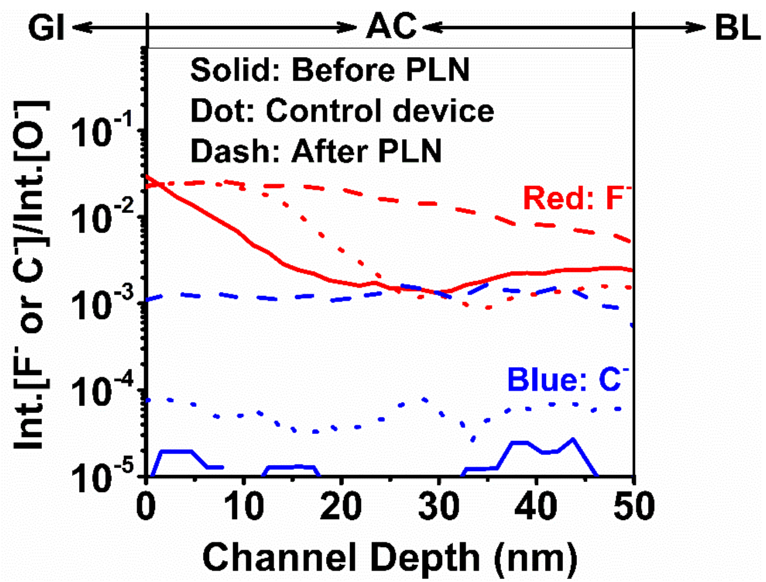
→ The PLN process is more efficient than conventional thermal annealing.

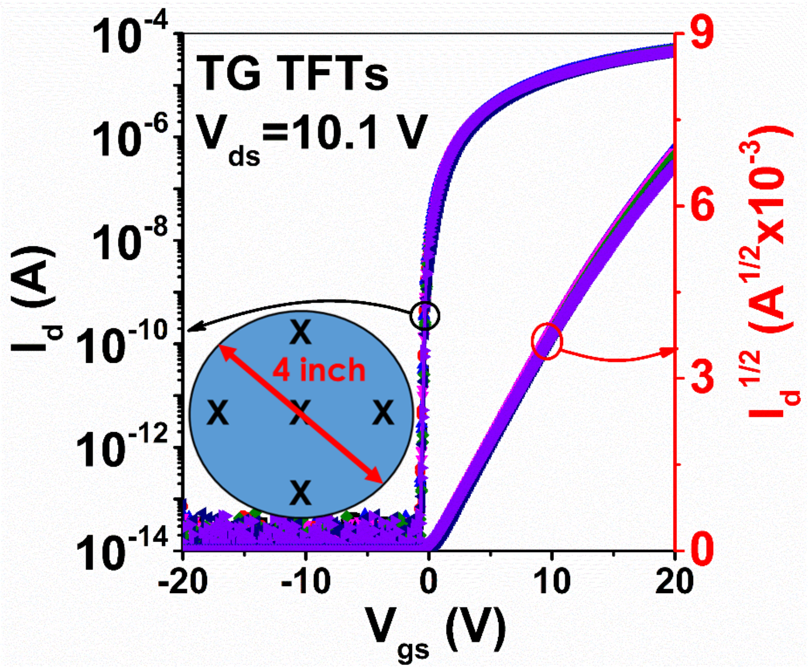
Unanticipated ΔV_{th} in TG MO TFTs after PLN (II)

- **Underlying mechanism & Device uniformity**



TOF-SMIS depth profiles of F^- and C^- in the AC of the TG MO TFTs





Key electrical parameters of 10 samples TG MO TFTs (after PLN) selected from the top, bottom, left, right, and center of a 4-inch glass wafer

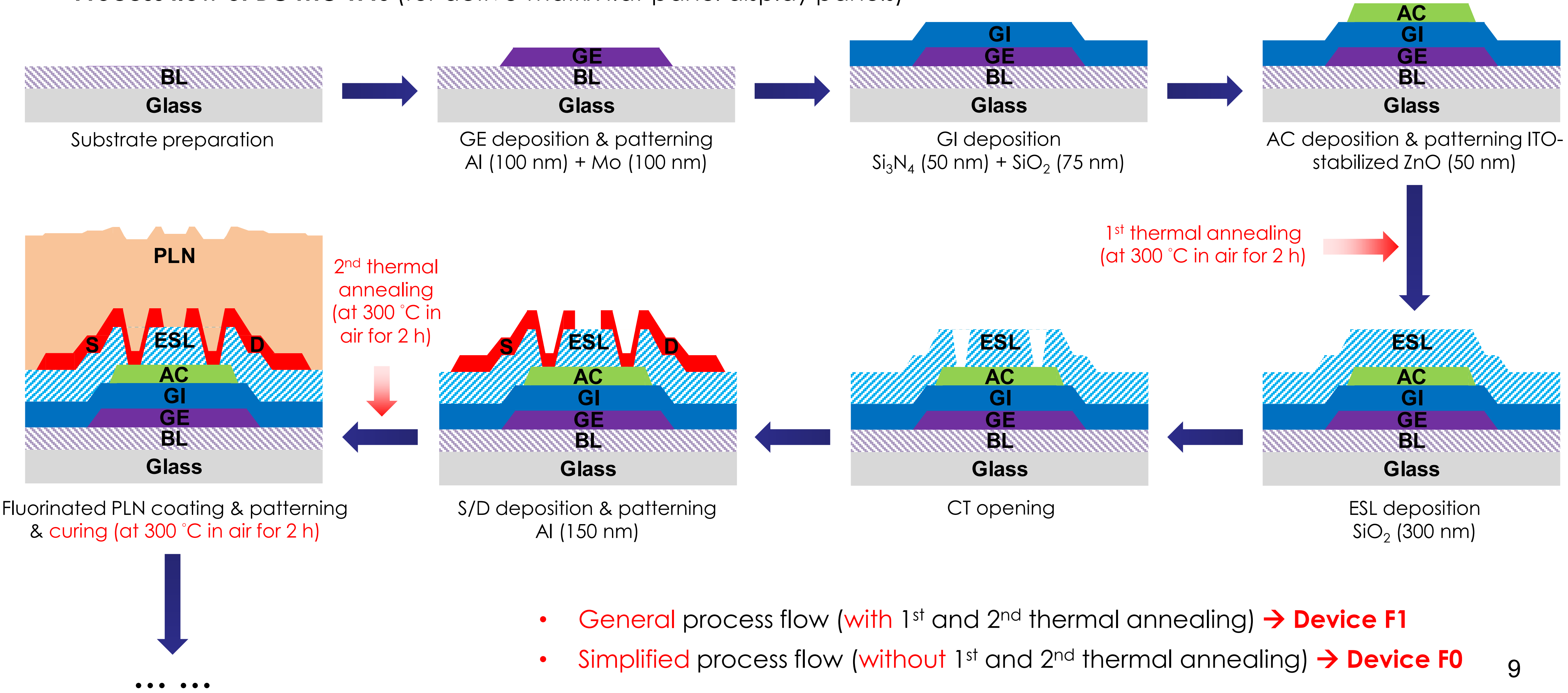
	μ_{sat} (cm^2/Vs)	V_{th} (V)	SS (mV/decade)	On-off ratio
Ave.	18.36	0.23	84.8	4.7×10^9
S.D.	0.56	0.20	0.9	1.5×10^8

- ✓ A larger ΔV_{th} → High fluorine and carbon content in the AC bulk → Fluorination treatment brought by PLN.
- ✓ Excellent electrical uniformity → An effective fluorination method for large-area displays and electronics.

? **TG MO TFTs → BG MO TFTs** (with no metallic GE between the PLN and the AC)

Fluorination Treatment on BG MO TFTs via PLN (I)

- **Process flow of BG MO TFTs** (for active-matrix flat-panel display panels)



Substrate preparation

GE deposition & patterning
Al (100 nm) + Mo (100 nm)

GI deposition
Si_3N_4 (50 nm) + SiO_2 (75 nm)

AC deposition & patterning ITO-stabilized ZnO (50 nm)

1st thermal annealing
(at 300 ˚C in air for 2 h)

ESL deposition
SiO_2 (300 nm)

CT opening

S/D deposition & patterning
Al (150 nm)

2nd thermal annealing (at 300 ˚C in air for 2 h)

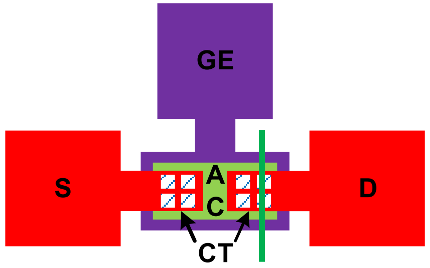
Fluorinated PLN coating & patterning & curing (at 300 ˚C in air for 2 h)

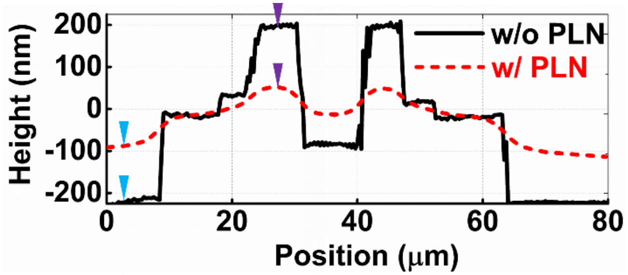
… …

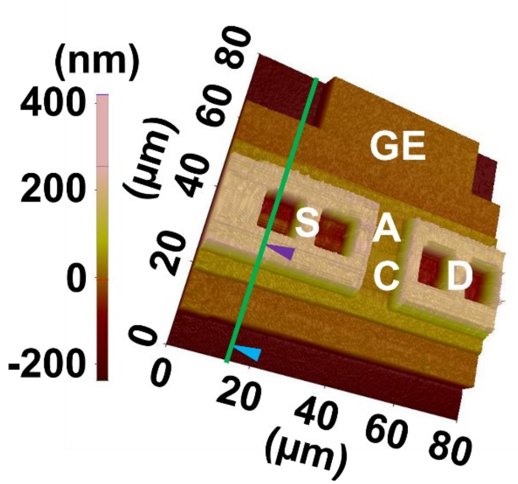
- General process flow (with 1st and 2nd thermal annealing) → **Device F1**
- Simplified process flow (without 1st and 2nd thermal annealing) → **Device F0**

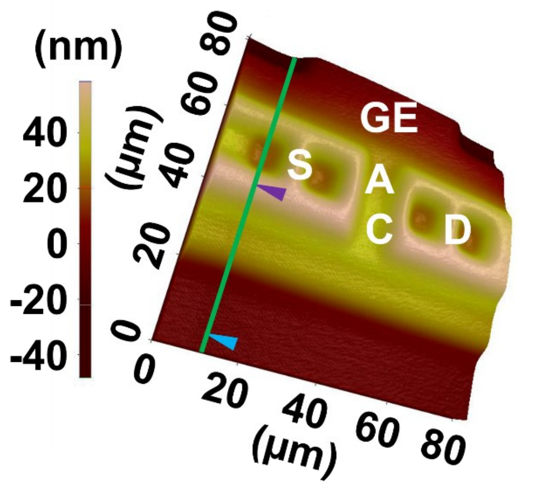
Fluorination Treatment on BG MO TFTs via PLN (II)

- **Planarization efficacy**



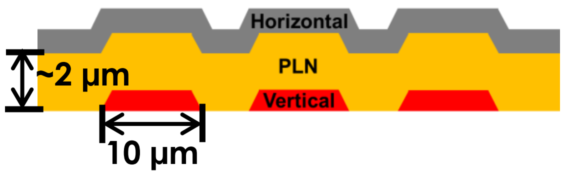


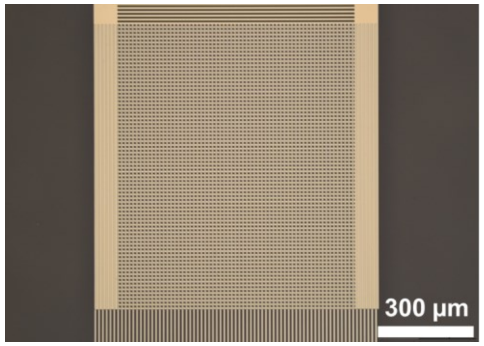


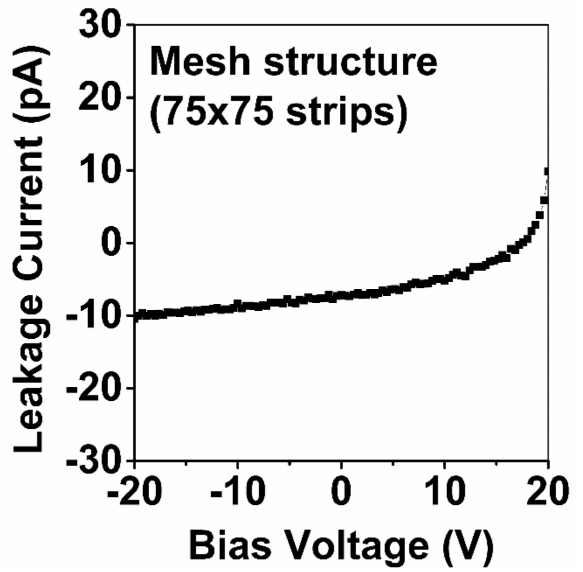


	Before PLN	After PLN
Max. height difference	423 nm	158 nm
RMS roughness	133 nm	43 nm

- **Insulation efficacy**







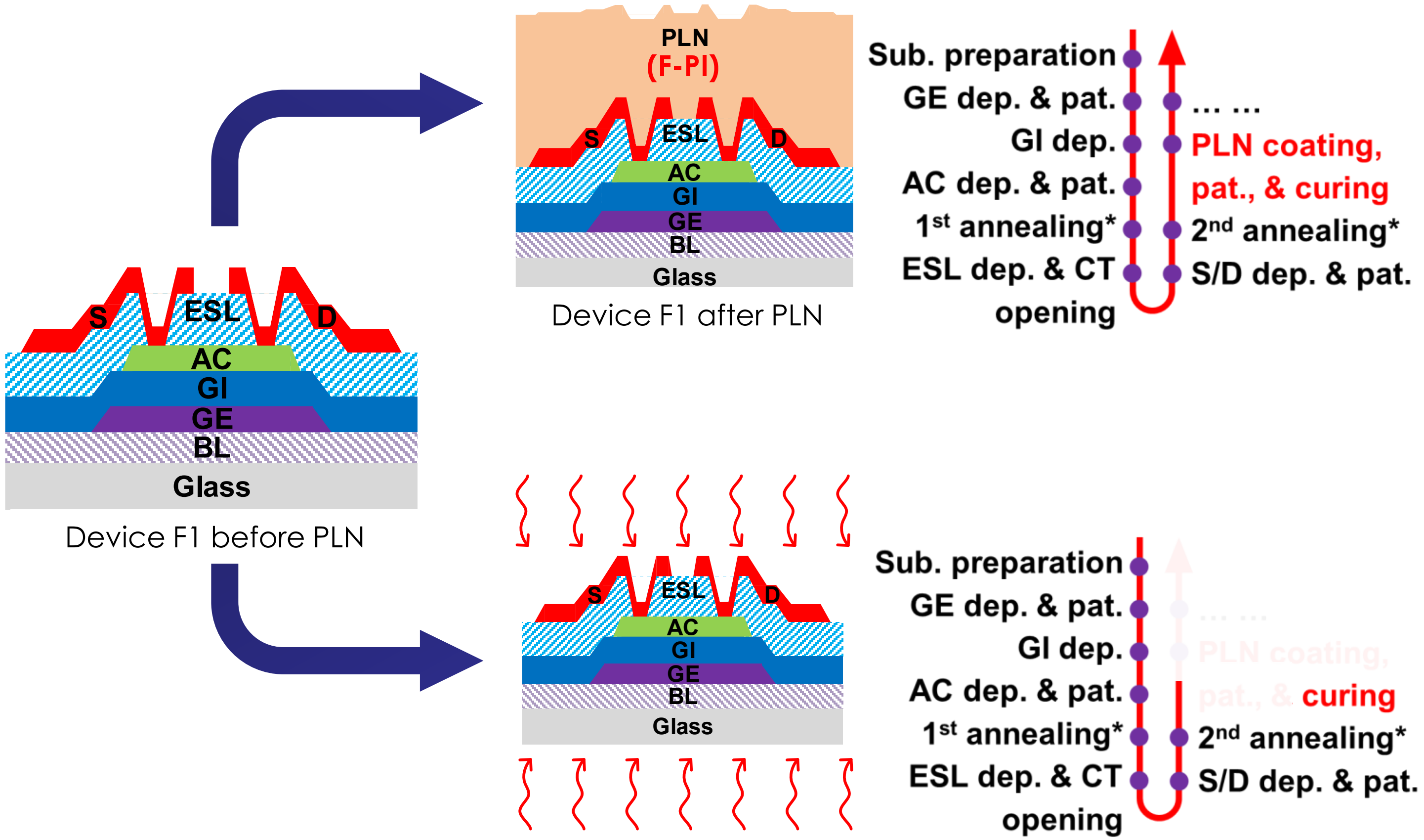
75 horizontal strips (200-nm-thick Mo)
by 75 vertical strips (150-nm-thick Al)

→ 11,250 sidewalls and 5,625 overlapped mesas (10 μm*10 μm)

✓ The fluorinated PLN layer has a good planarization and insulation properties and are applicable to general display applications.

Fluorination Treatment on BG MO TFTs via PLN (III)

- **Device F1 before PLN vs. after PLN**



Device F1 before PLN

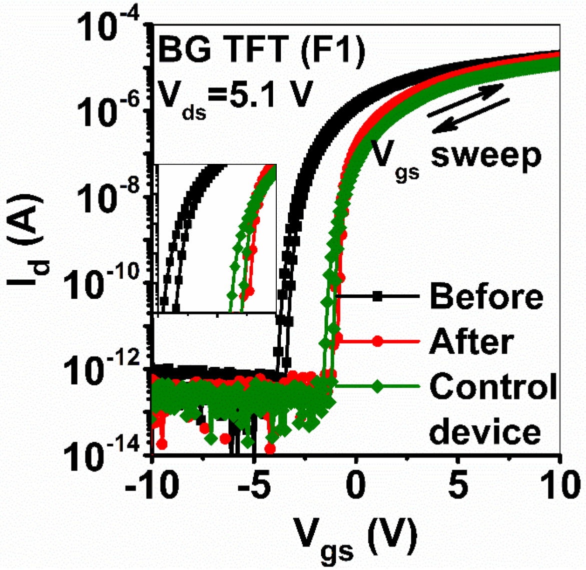
Device F1 after PLN

Control device F1*

Sub. preparation
GE dep. & pat.
GI dep.
AC dep. & pat.
1st annealing*
ESL dep. & CT opening
S/D dep. & pat.
2nd annealing*
PLN coating, pat., & curing
… …

Sub. preparation
GE dep. & pat.
GI dep.
AC dep. & pat.
1st annealing*
ESL dep. & CT opening
S/D dep. & pat.
2nd annealing*
PLN coating, pat., & curing
… …

Electrical performance of Device F1 before/after PLN and control device



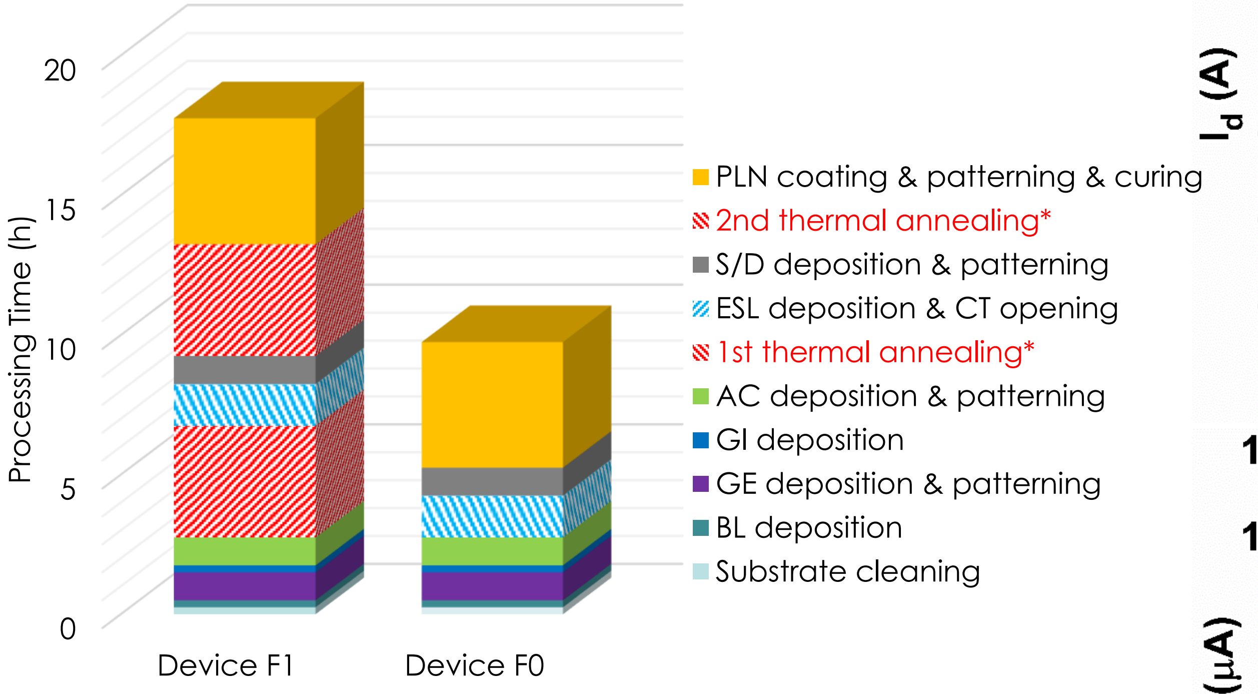
	Device F1 before PLN	Device F1 after PLN	Control Device F1*
V_{th} (V)	-3.3	-0.7	-1
ΔV_{th} (V)	-	2.6	2.3
Hysteresis (V)	~0.4	<0.1	~0.4
SS (mV/decade)	130.2	80.8	107.8

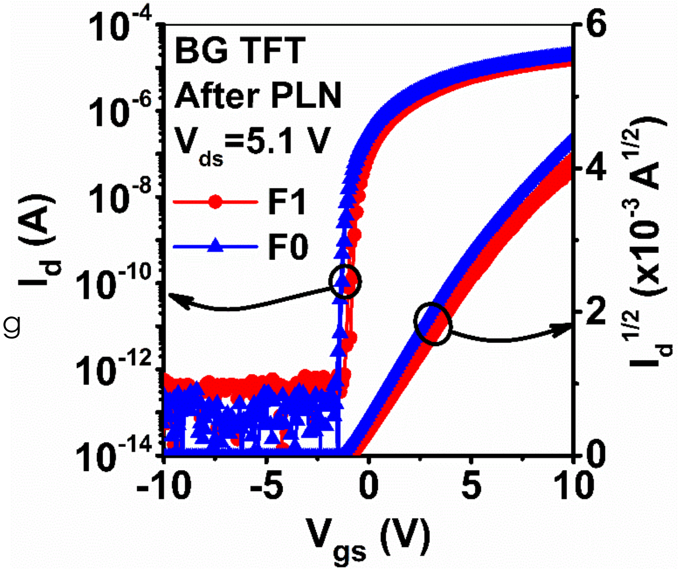
✓ The PLN process also works for improving the performance of BG MO TFTs.

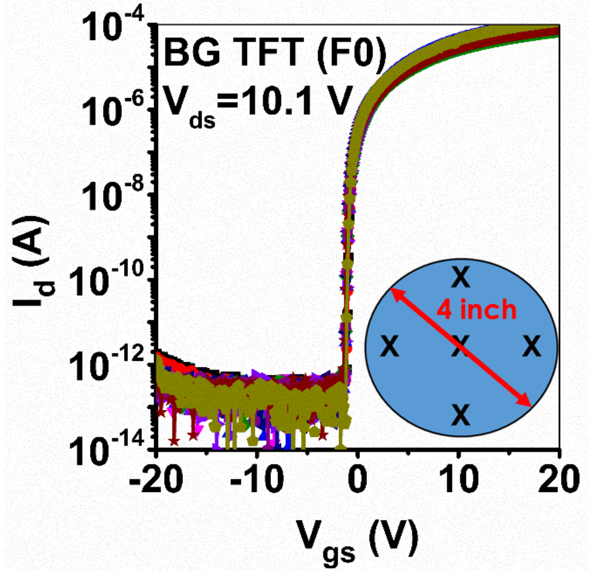
Fluorination Treatment on BG MO TFTs via PLN (IV)

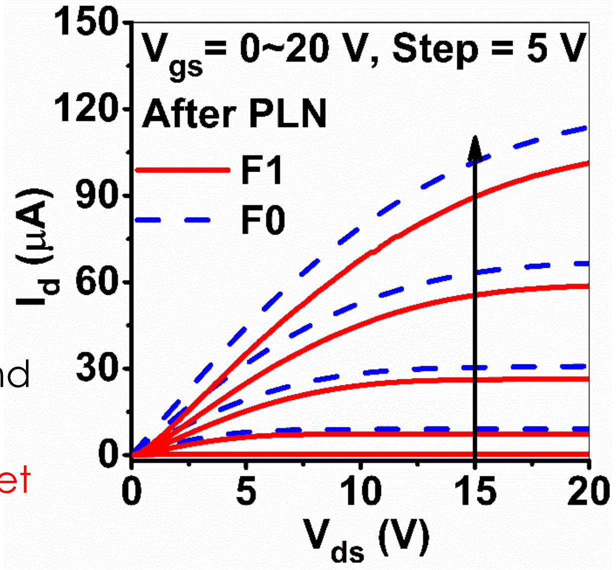
- **Device F1 vs. Device F0**

Estimated processing time of Devices F1 and F0









Key electrical parameters of Devices F1 and F0

	Device F1	Device F0
μ_{sat} (cm^2/Vs)	12.8	22.3
V_{th} (V)	-0.7	-0.8
On-off ratio	4.1×10^9	1.5×10^{10}
SS (mV/decade)	80.8	81.6

*Record low SS among fluorinated MO TFTs

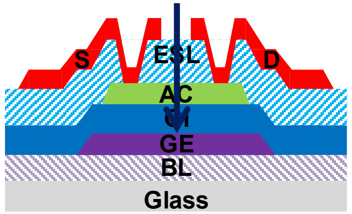
✓ Comparable and uniform electrical performance in Device F0

→ The PLN process itself is efficient to passivate defects and activate MO TFTs even with no need for annealing before PLN.

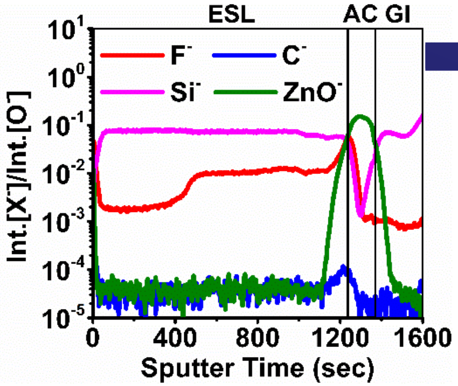
→ A shorter production cycle and a lower process thermal budget for more cost-effective manufacturing.

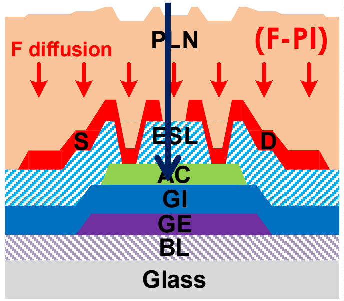
Fluorination Treatment on BG MO TFTs via PLN (V)

- **TOF-SIMS analysis in Device F0**

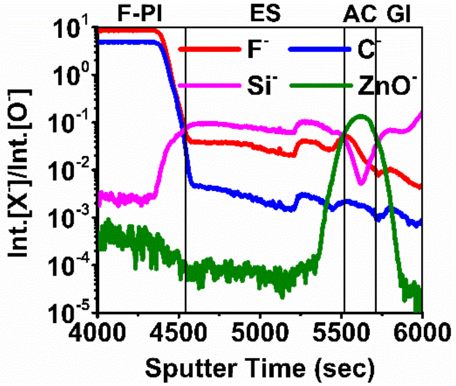


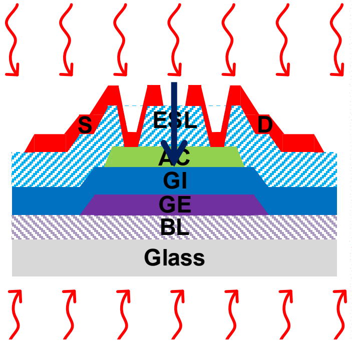
Device F0 before PLN



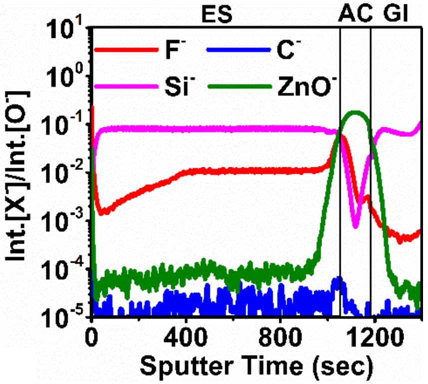


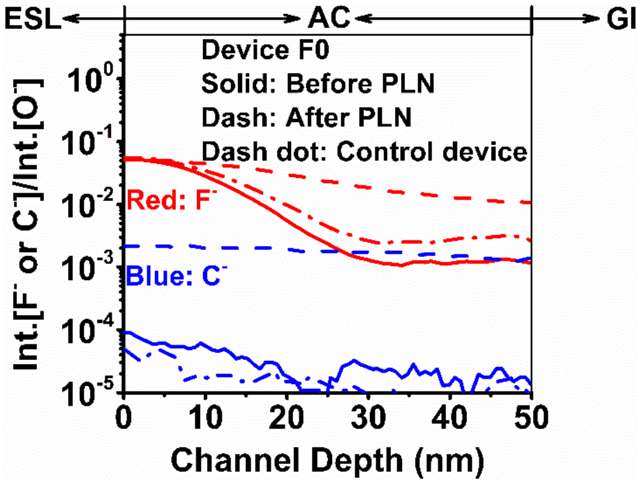
Device F0 after PLN





Control device F0*



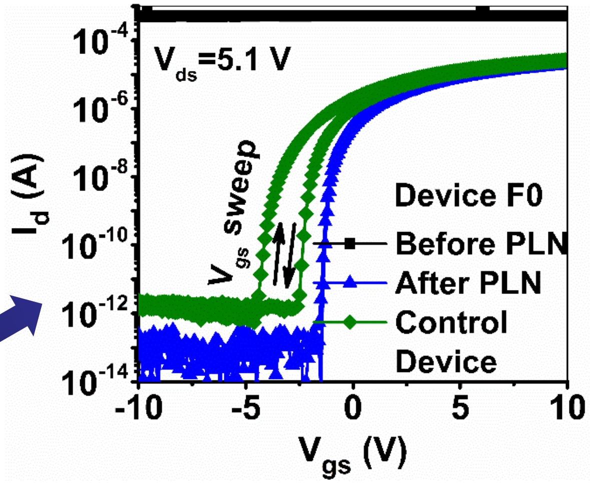


Similar F⁻ & C⁻ profiles

Diffusion of fragments like CF_x radicals from the F-PI PLN through the ESL into the AC

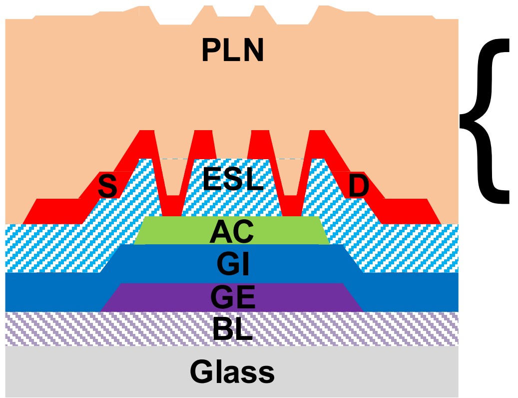
Oxygen vacancy passivation by F species

Improved performance



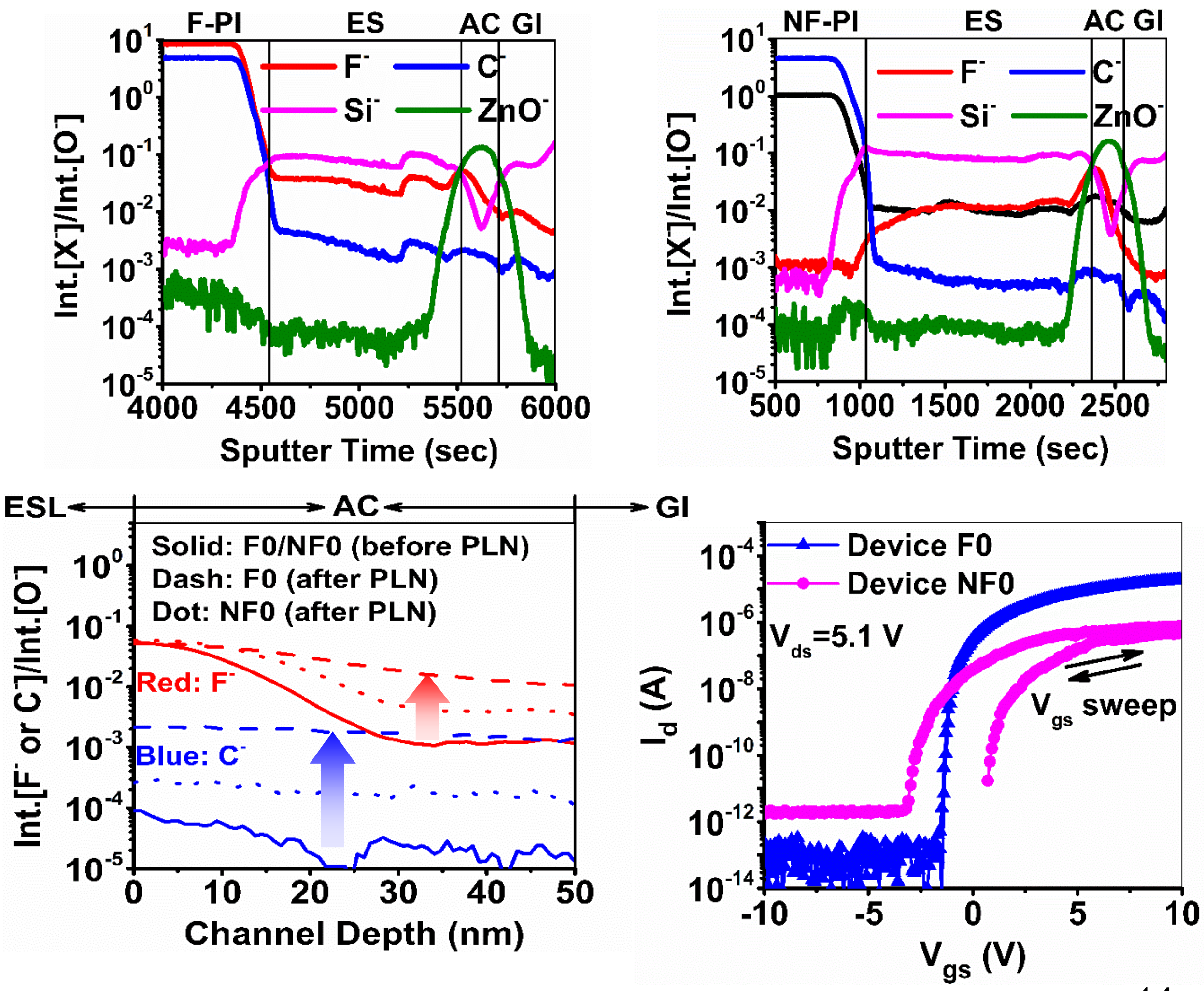
Fluorination Treatment on BG MO TFTs via PLN (VI)

- **Device F0 vs. Device NF0**



Fluorinated polyimide (F-PI) → **Device F0**

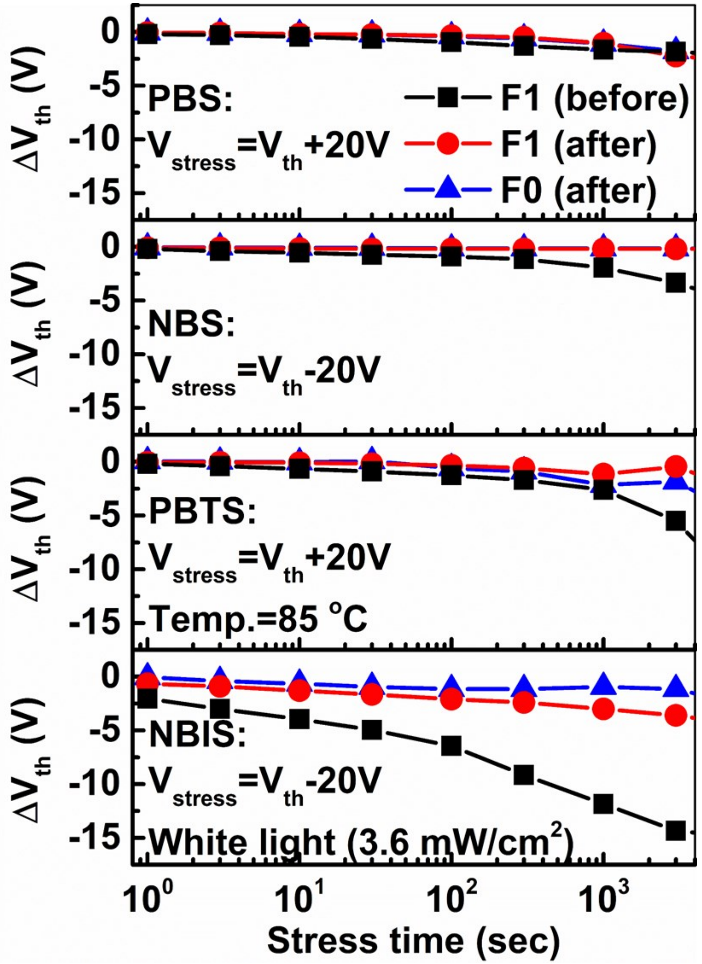
Non-Fluorinated polyimide (NF-PI) → **Device NF0**



- Fluorine and carbon mainly origins from the F-PI PLN.
- Increased carbon intensity in the AC of Device NF0 is helpless for performance improvement.
- ✓ A fluorinated PLN layer is the key, and performance improvement after PLN is attributed to a cost-effective fluorination treatment.

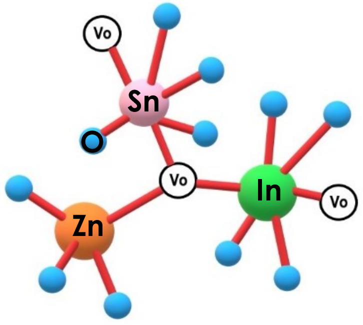
Fluorination Treatment on BG MO TFTs via PLN (VII)

- **Device stability against electrical, thermal, and illumination stresses**

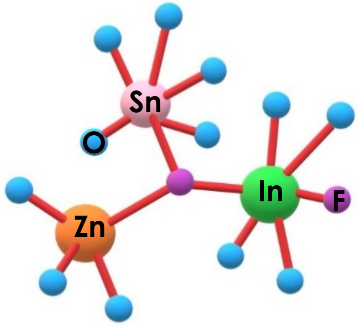


- After PLN, both F1 and F0 exhibit significantly improved stability.
- PBTS: $|\Delta V_{th}(F1)| < |\Delta V_{th}(F0)|$ ← more defects in Device F1 are compensated ← longer thermal annealing treatment for Device F1.
- NBIS: $|\Delta V_{th}(F1)| > |\Delta V_{th}(F0)|$ ← D_0(M-F)>D_0(M-O) ← more V_O are passivated by F ← Device F0 is not annealed before PLN.

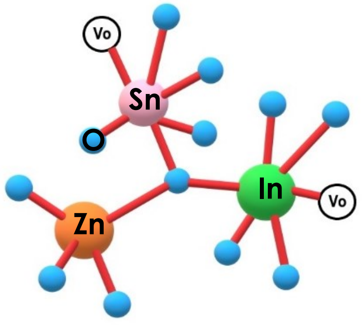
→ Fluorination treatment prior to oxidation treatment may lead to an enhanced illumination stability?



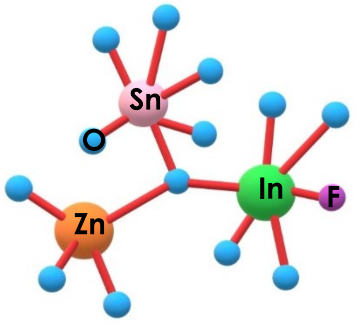
Device F0 before PLN



Device F0 after PLN



Device F1 before PLN



Device F1 after PLN

*The results of Device F0 before PLN is not shown because of short-circuit.

Conclusion

1. We demonstrate a PLN process using fluorinated polyimides that can improve the electrical performance of MO TFTs even without the need for additional thermal annealing steps.
2. The underlying mechanism is attributed to the diffusion of fluorine species from the PLN layer to the AC layer and the following defect passivation during the thermal curing of the F-PI.
3. Both TG and BG MO TFTs fabricated with the PLN process exhibit significantly enhanced electrical characteristics and stability.
4. This study provides a cost-effective fluorination method to reduce the thermal budget and shorten the production cycle in the fabrication of AM-FPD panels.

Thank you for your kind attention!

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